Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-18 are pending in this application, with 1, 8, and 15 being the independent claims.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,297,162 to Jang et al.("the Jang patent") in view of U.S. Patent 6,225,207 to Parikh ("the Parikh patent"). Applicant respectfully traverses this ground of rejection.

The Jang patent appears to teach a method to reduce silicon oxynitride etch rate in a silicon oxide dry etch. The silicon oxynitride is used as etching stop for silicon oxide plasma etching in the fabrication of an integrated circuit. The Jang patent makes no reference to the claimed process of fabricating a metal-insulator-metal capacitor.

The Parikh patent appears to teach a technique for triple and quadruple damascene fabrication, providing a fabrication method for integrated circuits that involves chemical etching. The Parikh patent makes no reference to the claimed process of fabricating a metal-insulator-metal capacitor.

Both the Jang and the Parikh patents disclose steps for depositing a substrate, a first dielectric layer, a stop layer, a second dielectric layer, and another subsequent stop layer and dielectric layers.

However, as the examiner points out that the Jang patent fails to disclose several steps of the claimed method to fabricate a metal-insulator-metal capacitor.

The Parikh patent discloses, in the sequence illustrated in FIG. 3A - 3F, a method to fabricate structures including a power line trench and two signal line trenches, wherein one of the signal line trenches has an underlying via hole. The steps of the process disclosed by the Parikh patent are: depositing a first dielectric on a substrate (illustrated in FIG. 3A); depositing a second dielectric layer on the first dielectric layer; subsequently depositing a third, forth, and fifth dielectric layers; depositing a first photoresist layer on the fifth dielectric layer.

The second and the forth dielectric layers are the stop-etch layers. The first photoresist layer is patterned by etching and stripped. A second photoresist layer is deposited on the fifth dielectric layer. The resist layer is patterned using a chemical etching process. As depicted in FIG. 3E, trenches 326 and 334 are deepened. Trench 334, denominated third opening, is etched until the stop layer 318, exposing the stop layer 318.

In contrast, step (h) of claim 1 recites "performing a further etching process, using the second patterned mask layer as a further etching mask, to etch the stop layer below the second opening and to partially etch a third opening adjacent the second opening in the second dielectric layer without exposing the stop layer thereunder." Thus, the Parikh patent does not teach this claimed step.

More over, there is no teaching in either cited patent that indicates that the described process is used for manufacturing a metal-insulator-metal capacitor, as recited in claim 1: "wherein a metal-insulator-metal (MIM) capacitor is formed by the first region of the first metal layer, the stop layer and the filled first opening, and the filled second opening forms a via between the first and second metal layers, and the first and second metal layers include copper."

The Jang and Parikh patents fail to teach or suggest all the steps of claim 1. Therefore, Applicant respectfully submits that claim 1 is patentable over the art of record. Further, claims 2 through 7 which depend from and add features to claim 1, are also patent able for at least the same reasons provided above.

Independent claim 8 recites a process for fabricating a metal-insulator-metal capacitor that involves the use/forming of a first, second and third patterned masking layer over the substrate. The Parikh patent specifically states in col. 5, line 42, that "The inventive techniques for fabricating triple and quadruple damascene structures described in the above embodiments advantageously require only two etch mask layers and need only one planarizing or etch back step to define the interconnect lines." As such, independent claim 8 is patent able over the art of record.

Independent claim 8 further recites a process that involves formation of a first and a second metal layers. The Parikh patent specifically states in col. 8, line 26 that "The three design rule patterns of the present invention require only two masks. Advantageously, the novel technique needs only a single metal fill for all three patterns and requires only one planarizing step, resulting in reduced fabrication costs as compared with conventional techniques."

For the reasons set forth for claim 1, and the above additional reasons, the Parikh patent fails to disclose all the elements of claim 8. As such, independent claim 8 is patent able over the art of record.

Claims 9 through 13, which depend from and add features to claim 8, are also patent able for at least the reasons addressed above.

Independent claim 15 discloses a process of manufacturing a metal-insulator-metal capacitor, forming its main components: the lower plate, the upper plate and the insulator. There is no reference in the Parikh patent to any of these elments nor to the concept of metal-insulator-metal capacitor. Accordingly, for at least the reasons set forth above in connection with claim 1, Applicant respectfully requests that the rejection of claim 15 also be withdrawn. Further, claims 16 and 18, which depend from claim 15, are also patent able over the art of record for at least the reasons addressed above..

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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Version with markings to show changes made

Materials such as doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion, regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), molybdenum (Mo), and refractory metal silicides [suicides] are examples of other conductors.